Optimization and Analysis of PwrSoC Buck Converter with integrated passives for Automotive Application

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***Abstract*— Current trends in automotive industry impose as main drivers the improvement of the efficiency and the miniaturization of the electronic systems. New technologies for passives enable the integration of the power converter together with the load in a single chip. This study is related to the optimization and analysis of a PwrSoC Buck converter system used to supply in-chip load for automotive application. Due to the complexity of the design and various constrains, multi-variable optimization is employed. Furthermore, this paper analyzes the impact of the used technologies on the system efficiency and provides information how to improve system efficiency.**

I. INTRODUCTION

Current trends in automotive industry [1] are showing significant increase of car electronics, shifting the functionality form mechanical to electrical systems. According to this study, during the period 1993-2008, vehicle production has increased by 44%, while the automotive electronic content has grown by 155% and the semiconductor content by 325%. These growing trends are imposing efficiency and miniaturization as main drivers for power supply system due to the mass and CO_2 reduction. On the other hand, different studies of the trends in power electronics [2]-[5] are showing that significant effort is invested in integration and miniaturization of the power system. Special effort is given to the implementation of the passives [6]-[10] and improvement of the semiconductor design and models for losses estimation [11]-[15].

Having in mind these current trends, the work presented in this paper is part of a project that proposes a fully integrated solution for an automotive power supply chain from the battery to the microcontroller. The system, presented in Fig. 1, is composed of the power converter and a load. The power converter can be implemented as a single stage solution or multistage, adapting the semiconductor technology depending on the selected solution. In order to optimize the power converter a multi-variable optimization needs to be employed. In this paper, the focus is on the single stage system, where a synchronous buck converter, presented in Fig. 2, is optimized under both static and dynamic constraints to comply with automotive qualification defined within the European project called PowerSwipe [16]. The

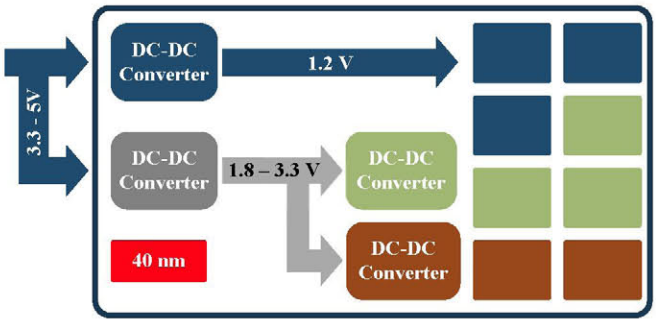

Figure 1. PwrSoC System implementation.

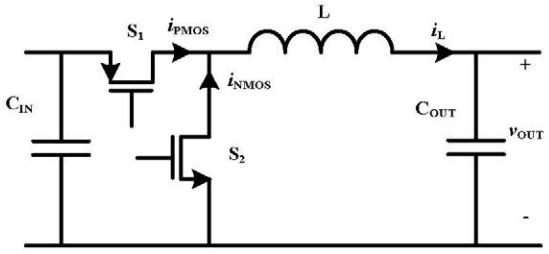

Figure 2. Single Phase Buck converter.

converter is designed using Infineon semiconductor technology, Tyndall inductor technology and IPDiA capacitor technology. In the first part of the paper the models used to estimate the losses are presented. The second part is dedicated to the algorithm used for optimization, where the algorithm is optimizing design variables to obtain maximal system efficiency at nominal operating point, satisfying both static and dynamic constraints imposed by the specification. Finally, the third part shows the obtained results.

II. MODELS

The component models are provided by manufacturers of the components or derived based on the simulations provided by the manufactures and they are used for the estimation of the power losses. On the other hand, the models of the control are based on the literature and can be divided as the switching model, implemented as a hybrid state-space model [17], and average model, implemented as a liner state-space model based on [18] for VMC and [19] for PCMC.

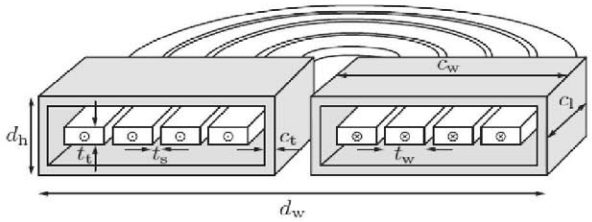

Figure 3. Cross-sectional view of the cored racetrack inductor with noncored half-spiral end turns.

A. Magnetics model

The magnetic components are designed using Tyndall National Institute technology. The components are based on "Magnetics on Silicon" process which is used for fabrication of micro-inductor and micro-transformer structures. The process is currently employed to fabricate 'elongated spiral' or 'racetrack' device structures, shown in Fig. 3. The geometrical parameters of the device are defined in Table I.

The analytical model of a basic inductor, validated by 2D FEA simulations, has been implemented based on the equation presented in [7]. The losses of the inductor are divided into DC conduction losses, $P_{L\_Cu\_DC}$, AC conduction losses, $P_{L\_Cu\_AC}$, core hysteresis losses, $P_{L\_Fe\_Hyst}$, and core eddy-current losses, $P_{L\_Fe\_Eddy}$. The inductor conduction losses are estimated using the inductor DC resistance, R_{DC}, and AC resistance factor for kth switching frequency harmonic, F_k, therefore the conduction losses are calculated by

$$P_{L\_Cu\_DC} = R_{DC} I_{L\_DC}^2, \tag{1}$$

$$P_{L\_Cu\_AC} = R_{DC} \sum_{k=1}^{k_{max}} F_k \frac{I_{Lk}^2}{2}, \tag{2}$$

where I_{L_DC} is the DC inductor current and I_{Lk} is the amplitude of the inductor current kth switching frequency harmonic.

The core losses, both hysteresis and eddy-current losses are calculated under the assumption that both the magnetic field and flux density are constant throughout the core. Their DC values are calculated using

$$H_{DC} = \frac{N I_{L\_DC}}{2(c_w + d_h)}, \tag{3}$$

$$B_{DC} = \mu_0 \mu_C H_{DC}. \tag{4}$$

The inductor core hysteresis losses, created due the hysteretic dependence of the flux density (B) versus magnetic field (H), are calculated using

$$P_{L\_Fe\_Hyst} = K_h f_{SW} \left(\frac{\Delta B_{PP}}{2} \right)^b V_C, \tag{5}$$

where K_h and b are material dependent parameters, V_C is the core volume, f_{SW} is the switching frequency and ΔB_{PP} is peak to peak flux density. calculated using $\Delta B_{PP} = B_{DC} \cdot \Delta I_{L\_PP} / I_{L\_DC}$.

TABLE I. GEOMETRICAL PARAMETERS DESCRIBING THE CORED RACETRACK INDUCTOR

Symbol	Description
N	Number of turns
t_W	Winding width
t_t	Winding thickness
t_S	Winding spacing
c_W	Core width
c_t	Core thickness
c_l	Core length
d_h	Device height
d_W	Device width
d_l	Device length

The eddy-current losses of the magnetic core are calculated by using proximity losses estimation. By assuming that the eddy-currents are generated due to the proximity effect of generated magnetic field in the core, the losses are calculated using

$$P_{L\_Fe\_Eddy} = 4 \frac{\rho_C (c_w + d_h) c_l}{c_t} \sum_{k=1}^{k_{max}} v_k \frac{\sinh(v_k) - \sin(v_k)}{\cosh(v_k) - \cos(v_k)} H_k^2, \tag{6}$$

where ρ_C is the core resistivity and H_k is the magnetic field amplitude at kth harmonic and it can be calculated using $H_k = H_{DC} \cdot I_{Lk} / I_{L\_DC}$. The parameter v_k is the core thickness (c_t) to core skin depth ($\delta_{c,k}$) ratio at the kth switching frequency, defined by

$$v_k = \frac{c_t}{\delta_{c,k}} = \frac{c_t}{\sqrt{\frac{\rho_c}{\mu_0 \mu_C \pi k f_{SW}}}}. \tag{7}$$

The inductor is connected to the rest of the converter with thought-silicon vias (TSV) on both terminals, generating additional losses. The inductor TSVs are modeled as series impedance composed of a resistance R_{Lpar} and an inductance L_{Lpar}, which is added to the total impedance of the inductor. The additional losses component, P_{Lpar}, is calculated using inductor current RMS value:

$$P_{Lpar} = R_{Lpar} I_{L\_RMS}^2. \tag{8}$$

B. Capacitor model

The capacitors are designed using IPDiA low voltage MOSAIC PICS3 capacitor technology presented in Fig. 4a. Furthermore, in Fig. 4b the dependence of equivalent series resistance ESR on desired capacitance is presented. It can be seen that ESR•C product is not constant and that for bigger values of capacitance the product increases. In other words, the zero of the capacitor, defined by the ERS and C goes down on the lower frequencies thus influencing the converter dynamic behavior. Moreover, the losses of the capacitor do not reduce linearly with increase of capacitance. Thus in order to improve behavior, capacitor model has been developed based on a basic capacitor blocks with low

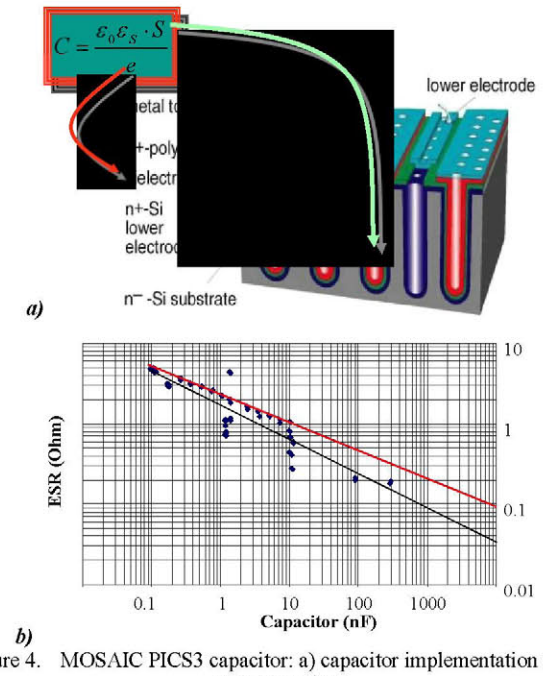

Figure 4. MOSAIC PICS3 capacitor: a) capacitor implementation and b) ESR·C product.

capacitance, presented in Fig. 5. Doing so, constant ESR•C product is maintained, so the dominate zero is kept on higher frequencies and the losses reduce linearly with the capacitance.

In order to generate desired capacitance C_{OUT}, the basic building blocks are put in parallel in that manner that minimal number of cells is used. The blocks are defined for a cell of 12 nF, 3.6 nF and 1.6 nF, as shown in Fig. 5. Each cell is designed to occupy the same silicon area, penalizing density while improving performance. The equivalent capacitance, C_{eq}, series resistance, ESR, and inductance, ESL, are calculated as parallel connections of each block capacitances, resistances and inductances, respectively:

$$C_{eq} = N_{12n}C_{12n} + N_{3n6}C_{3n6} + N_{1n6}C_{1n6}, \quad (9)$$

$$ESR = \frac{R_{12n}}{N_{12n}} || \frac{R_{3n6}}{N_{3n6}} || \frac{R_{1n6}}{N_{1n6}}. \quad (10)$$

$$ESL = \frac{L_{12n}}{N_{12n}} || \frac{L_{3n6}}{N_{3n6}} || \frac{L_{1n6}}{N_{1n6}}. \quad (11)$$

The losses are calculated using capacitor RMS current, I_{C_RMS}, and equivalent ESR:

$$P_{C\_ESR} = ESR \cdot I^2_{C\_RMS}. \quad (12)$$

Similarly as in the case of the inductor, both the input and the output capacitors are connected to the rest of the converter with TVSs at both terminals. The TVS is, once again, modeled as series impedance composed of a resistance R_{Cpar} and an inductance L_{Cpar}, which is added to the total impedance of the capacitor. The additional losses component, P_{Cpar}, is calculated using capacitor current RMS value:

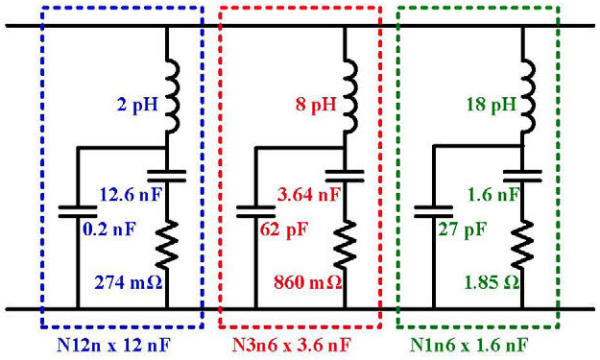

Figure 5. Basic capacitor cells: 12 nF (blue), 3.6 nF (red) and 1.6 nF (green) basic building blocks.

$$P_{Cpar} = R_{Cpar} I^2_{C\_RMS}. \quad (13)$$

C. Semiconductor model

The semiconductors used in LV-DCDC converter are implemented using Infineon MOSFET technology. The model is presented in [20] and consists of nine functions, three static characteristics and five dynamic characteristics:

1. NMOS body diode voltage drop,
2. NMOS on-resistance,
3. PMOS on-resistance,
4. NMOS gate charge,
5. PMOS gate charge,
6. NMOS body diode reverse-recovery energy loss,
7. PMOS turn-off energy loss,
8. PMOS turn-on energy loss.

The modeling functions based on discrete number of simulations performed by Cadence, where the input variables are MOSFET width w and current I. The modeling functions are obtained by interpolating the output variable using linear plains as presented in Fig. 6. After the measurements are obtained (Fig. 6a), for each four points are the intermediate point is defined (Fig. 6b) which is used to create output linear plains (Fig. 6c). In the case that a function is defined with three input variable (e.g. the on resistance), the third variable is declared as a parameter and interpolation is performed, once again, using the MOSFET width and the MOSFET current.

Obtaining all needed functions, power losses of semiconductors can be calculated based on the waveforms of the MOSFETs currents, shown in Fig. 7, using the equations presented in TABLE II, where w_P and w_N are widths of PMOS and NMOS, respectively; V_{GSP} and V_{GSN} are gate to source voltage of PMOS and NMOS, respectively; I_L, I_0 and I_1 are mean, minimal and maximal inductor currents, respectively; I_{Pmos_eff} and I_{Nmos_eff} are PMOS and NMOS RMS currents, respectively; f_{SW} is converter switching frequency; T_{SW} is converter switching period; D is duty-cycle; t_{dead_N2P} and t_{dead_P2N} are dead-times at 0 (T_{SW}) and DT_{SW}, respectively; R_{PMOS} and R_{NMOS} are on-resistance calculation functions of PMOS and NMOS, respectively; Q_{PMOS} and Q_{NMOS} are one-switching gate-charge calculation functions of PMOS and NMOS, respectively; $E_{PMOStum-on}$ and $E_{PMOStum-off}$ are

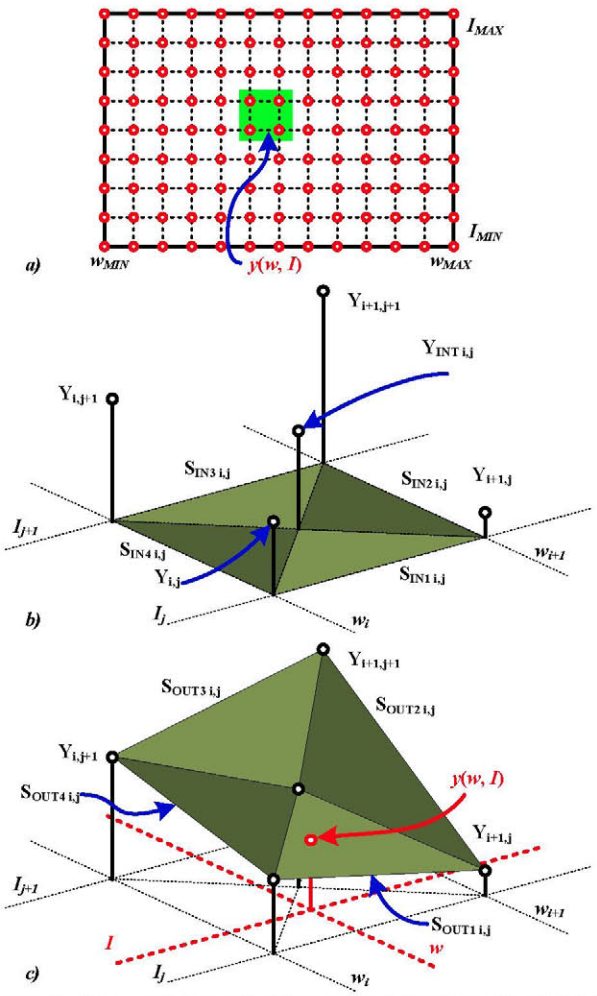

Figure 6. Basic modeling cell: a) Input plain defined by w[i] and I[j]; b) interpolation between four input points, input sub-domains, intermediate point $Y_{INT\,i,j}$; and c) the output plains and calculation *of* $y(w,I)$.

turn-on and turn-of one-switching energy-loss calculation functions of PMOS; $E_{Nrev\text{-}rec}$ is body diodes reverse-recovery one-switching energy-loss calculation function; $V_{D\text{-}NMOS}$ is NMOS body-diode voltage drop calculation function; P_{PMOS_Cond} and P_{NMOS_Cond} are PMOS and NMOS conduction power losses, respectively; P_{PMOS_gate} and P_{NMOS_gate} are PMOS and NMOS driving power losses, respectively; $P_{PMOS\_turn\_on}$ and $P_{PMOS\_turn\_off}$ are turn-on and turn-of losses of PMOS; $P_{NMOS\_rev\_rec}$ is NMOS body diode reverse-recovery power loss and P_{Ndiode_N2P} and P_{Ndiode_P2N} are dead-times losses at 0 (T_{SW}) and DT_{SW}, respectively.

The model has been explained in detail and validated in [20], where is demonstrated that the standard deviation of the model is 2.12 mW for the output power range from 60 mW to 600 mW, or that the relative standard deviation of the model is 1.89% for the same output power range. The relative errors are obtained by normalizing to the output power.

In order to estimate complete power losses of the converter, firstly, all needed waveforms are obtained using closed-loop hybrid state-space model presented in [17],

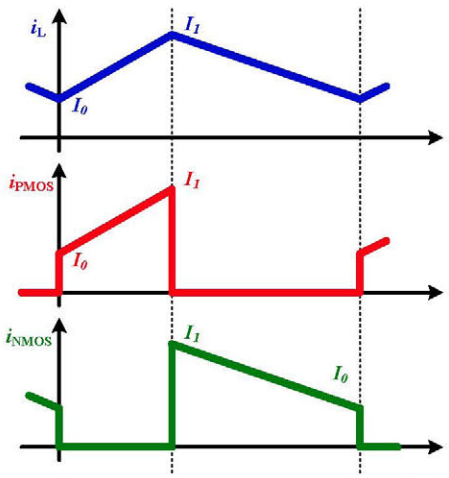

Figure 7. Buck converter currents: inductor current i_L (blue), PMOS current i_{PMOS} (red) and NMOS current i_{NMOS} (green).

TABLE II. CALCULATION OF SEMICONDUCTOR LOSSES

Losses component	Time instance	Equation
P_{PMOS_Cond}	-	$R_{PMOS}(w_P, V_{GSP}, I_L) \cdot I_{PmosRMS}^2$
$P_{PMOS\_turn\_on}$	0, (T_{SW})	$E_{PMOSturn\text{-}on}(w_P, I_0) \cdot f_{SW}$
$P_{PMOS\_turn\_off}$	DT_{SW}	$E_{PMOSturn\text{-}off}(w_P, I_1) \cdot f_{SW}$
P_{PMOS_gate}	0, (T_{SW})	$Q_{PMOS}(V_{GSP}, w_P, I_0) \cdot V_{GSP} \cdot f_{SW}$
P_{NMOS_Cond}	-	$R_{NMOS}(w_N, V_{GSN}, I_L) \cdot I_{NmosRMS}^2$
P_{NMOS_gate}	DT_{SW}	$Q_{NMOS}(V_{GSN}, w_N, I_1) \cdot V_{GSN} \cdot f_{SW}$
$P_{NMOS\_rev\_rec}$	0, (T_{SW})	$E_{Nrev\text{-}rec}(w_N, I_0) \cdot f_{SW}$
P_{Ndiode_N2P}	0, (T_{SW})	$I_0 \cdot V_{D\text{-}NMOS}(w_N, I_0) \cdot f_{SW} \cdot t_{dead\_N2P}$
P_{Ndiode_P2N}	DT_{SW}	$I_1 \cdot V_{D\text{-}NMOS}(w_N, I_1) \cdot f_{SW} \cdot t_{dead\_P2N}$

following the calculation of the semiconductors losses using equations form TABLE II. Passive losses are estimated using the equations presented in previous chapters.

III. OPTIMIZATION ALGORITHM

The optimization algorithm is searching for a set of input variables (the switching frequency f_{SW}, inductor area A_L, inductance L, output and input capacitance C_{OUT} and C_{IN} and widths of MOSFETs w_P and w_N) to obtain maximal efficiency at nominal operating point defined by typical output current I_{TYP}, output voltage V_{OUT} and input voltage V_{IN}. During the optimization process, static and dynamic behavior of the system are simulated to verify that both static and dynamic constraints are satisfied under the worst case steady-state operation and under the load steps and input voltage steps transients.

The algorithm is presented in Fig. 8, where it can be seen that the optimization is performed in two steps: in the first it performs coarse exhaustive search of the design space obtaining intermediate optimal point (OPT_{INT}), following by the second fine gradient search from that point to the optimal design (OPT). During the first part of the algorithm, the design space is searched with relatively large step in order to avoid local maximums in efficiency. The algorithm starts by defining current switching frequency $f_{SW}(k_F)$, the inductor area $A_L(k_{AL})$, and the inductance $L(k_L)$. If the inductor

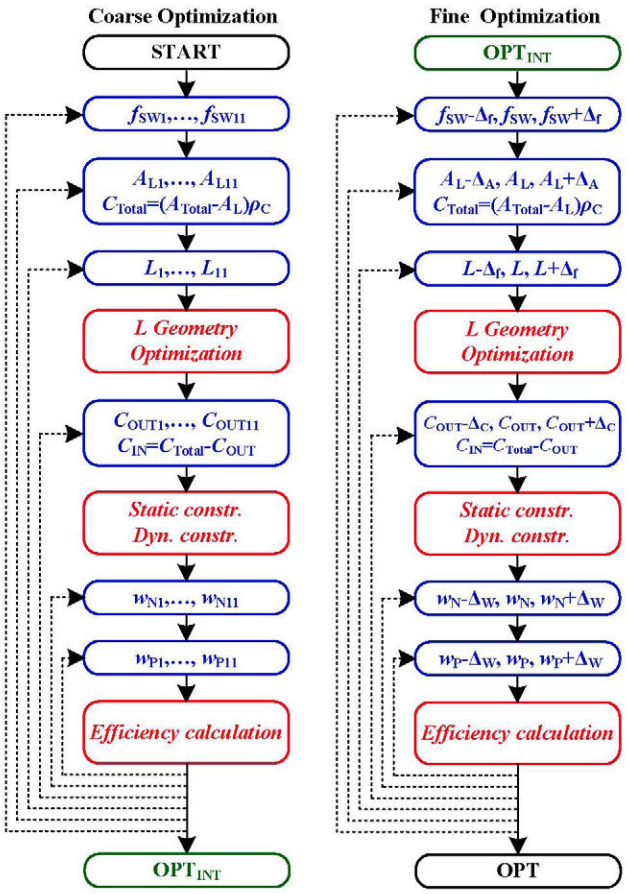

Figure 8. Optimization Algorithm.

implementation is possible, the optimal design is passed downwards and the algorithm selects the current output capacitor $C_{OUT}(k_C)$ and indirectly the input capacitor $C_{IN}(k_C)$, which is defined by difference of the total implementable capacitance C_{Total} and current output capacitance $C_{OUT}(k_C)$. the total implementable capacitance C_{Total} is defined by the capacitance density and an available capacitor area, obtained as the difference of the total area of the device and current inductor area $A_L(k_{AL})$. Obtaining all electrical parameters, $L(k_L)$, $C_{OUT}(k_C)$, $C_{IN}(k_C)$ and $f_{SW}(k_F)$, the converter is simulated both in steady-state and under transients. If the obtained performance satisfies the constrains of the system, the algorithm selects current NMOS and PMOS widths, $w_N(i_{WN})$ and $w_P(i_{WP})$, and estimates efficiency at typical operating point. After calculating all the possible combinations, the intermediate optimal design OPT_{INT} is obtained.

The second part of the algorithm is implemented as a gradient search: for each variable x, the efficiency is estimated in points x-Δx, x, x+Δx. The initial step, Δx is equal to the half of the step in the exhaustive search. If the efficiency is increased for one of the new designs in any direction, the new design is taken as the optimal and the process is repeated. If there is no increase in the efficiency, all the steps are reduced by half and the process is repeated. The algorithm stops when all of the steps are smaller than their corresponding precisions, P_X, defined by the user.

IV. Results and Discussion

In this chapter results of the optimization are presented and analyzed. The buck converter has been optimized to convert the input voltage V_{IN} of 5 V to the output voltage V_{OUT} of 1.2 V, operating with the typical current I_{TYP} of 280 mA and the maximum current I_{MAX} of 500 mA. Static peak to peak output and input voltage ripples are limited to 60mV and 250mV, respectively, while the maximum peak to peak output voltage deviation is 144 mV under the load steps of 50 mA and 300 mA with settling times of 2 ns and 2 µs, respectively, and input voltage step of 250 mV. The inductor peak to peak current ripple has been limited to 500 mA, while the inductance is limited to 2 µH. Total passives available area is 13 mm^2.

In order to evaluate impact of technologies used to design the system, a sweep of switching frequency for four different optimizations scenarios has been performed. The first scenario shows an impact of the inductor technology by performing the sweep in the switching frequency with ideal MOSFETs (without losses). In the second scenario, the inductor is assumed ideal (without losses and zero area for any value of inductance), while the MOSFETs are optimized for each switching frequency, showing an impact of Si technology on the system. In the third scenario, the MOSFETs are real, while the conduction losses are added to the inductor. Finally, in the fourth scenario, both MOSFETs and the inductor are real, showing the tendencies of the design behavior on the switching frequency.

The first optimization sweep is done on the system with real inductor and ideal, lossless switches, as commented above. The results of the optimizations are presented in Fig. 9. Is it can be seen in Fig. 9a), the total inductor power losses (blue, squares), thus the converter power losses, reduce as the switching frequency increases. The reason for this behavior can be found in Fig.9b), where components values are presented (the inductance L (black, triangles, up), the output capacitor C_{OUT} (red, circles) and the input capacitor C_{IN} (green, triangles, down)) and in Fig. 9c) where its corresponding areas are shown. When the system is operating at low switching frequencies, the operating conditions impose large values of the inductance and output capacitor capacitance to satisfy the specification. Since the capacitor area is proportional to the value of the capacitance, the inductor available area is drastically reduced (~5mm^2 at 2 MHz – see Fig.9c). Small available inductor area and big inductance penalize the inductor design since the number of turns needs to be high with narrower strips increasing the DC resistance and DC conduction losses (see Fig. 9a – black, triangles, up). In addition, the eddy-current losses are increased (purple, diamonds) since the core thickness is bigger to achieve needed core volume. On the other hand, when the system is optimized to operate at higher switching frequencies, needed component values are drastically decreased (L = 115 nH, C_{OUT} = 302 nF and C_{IN} = 321 nF) which facilitates integration of the inductor (inductor area is

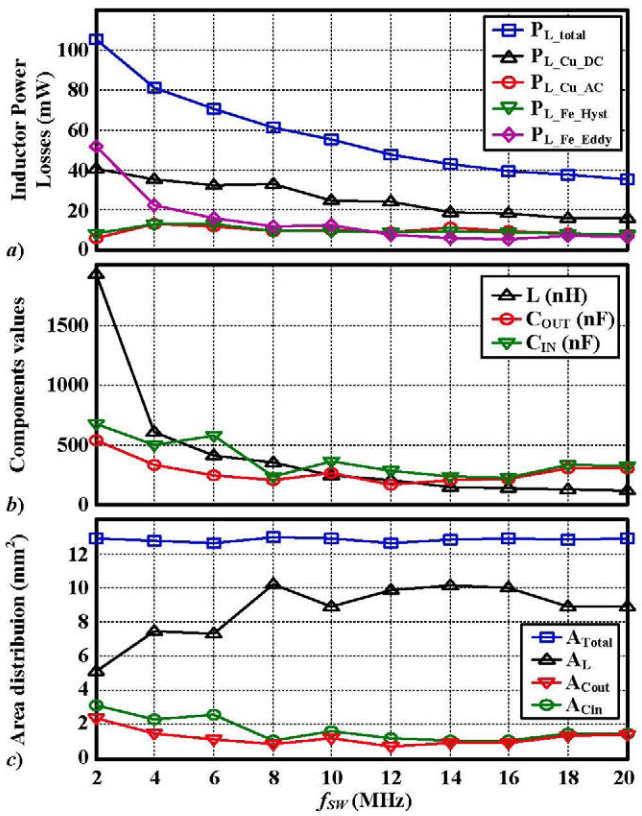

Figure 9. Ideal MOSFETs - Real Inductor: *a*) Breakdown of the inductor losses; *b*) Component values; *c*) Area distribution.

A_L = 8.88 mm^2). Under those conditions, wider strips can be used reducing conduction losses ($P_{L\_Cu\_DC}$ = 15.42 mW and $P_{L\_Cu\_AC}$ = 7.23 mW), while at the same time, smaller core thickness is needed to achieve the core volume, thus reducing core losses ($P_{L\_Fe\_Hyst}$ = 7.55 mW and $P_{L\_Fe\_Eddy}$ = 4.43 mW). Analyzing the losses distribution in the whole frequency range, it can be seen from Fig. 9a) that for each switching frequency, frequency dependent losses ($P_{L\_Cu\_AC}$, $P_{L\_Fe\_Hyst}$ and $P_{L\_Fe\_Eddy}$) are equal to the DC losses ($P_{L\_Cu\_DC}$).

The second optimization sweep is done on the system with ideal lossless inductor and real switches and the losses breakdown as well as the total losses are shown in Fig. 10. As expected, total losses (P_{total} - blue, square) increase due to the increase of the switching losses (P_{PMOS_sw} - red, circles; P_{NMOS_sw} - purple, diamonds), which are dominant with the respect to the conduction losses. Since the inductor is costless, the inductance converges to maximal available value (2 μH) reducing RMS currents in the system. Analyzing the losses distribution in the whole frequency range, it can be seen from Fig. 10 that for each switching frequency, the losses are equally distributed between PMOS losses (P_{PMOS_tot} - black, triangles, up) and NMOS losses (P_{NMOS_tot} - green, triangles, down).

The third optimization sweep is showing the impact of adding losses in the inductor. Starting from previous case with real switches and lossless inductor (Fig. 10), first, the winding losses are added to the system as shown in Fig. 11. The breakdown of the system losses are shown in Fig. 11a),

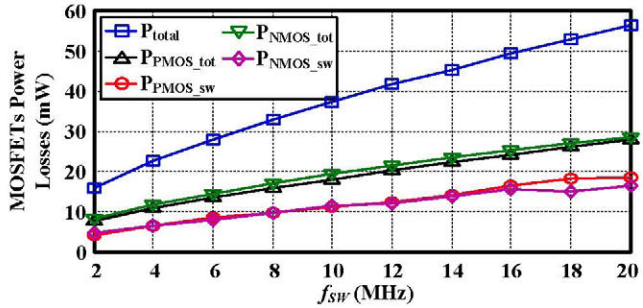

Figure 10. Real MOSFETs - Ideal Inductor: Breakdown of the MOSFETs losses.

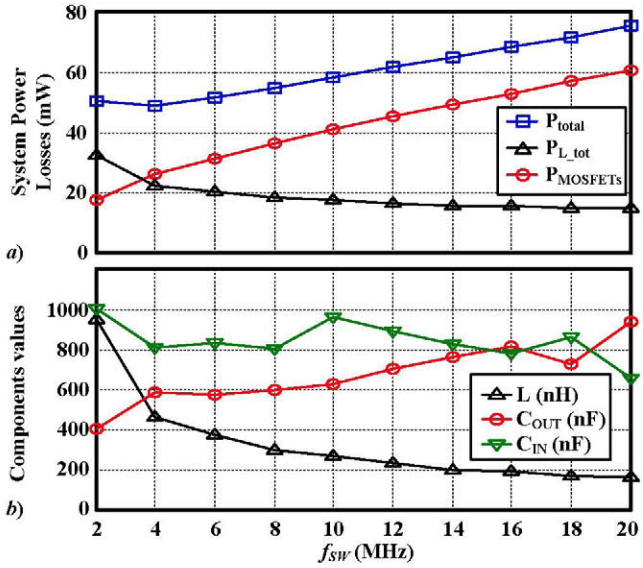

Figure 11. Real MOSFETs – Inductor with Cu losses: *a*) Breakdown of the converter losses; *b*) Component values.

where it can be seen that both total MOSFETs losses ($P_{MOSFETs}$ – red, circles) and total inductor losses (P_{L_tot} – black, triangles, up) have the same tendencies as presented in previous cases: the MOSFETs losses increase as the switching frequency increases, while the inductor losses are decreasing. The total losses have the minimum at 4 MHz where the losses are balanced between MOSFETs and the inductor. Fig 11b) presents components values, where can be seen, once again that the inductor inductance have the same tendency as in the first scenario. The difference between the newly obtained values and in the previous case originate from the fact that the core losses are ignored, thus the same inductance can be implemented in smaller area at the cost of the core thickness.

The fourth scenario analyses the converter with both real MOSFETs and the inductor, thus it represents the real system frequency sweep and the results are presented in Fig. 12 and Fig. 13. The Fig. 12 shows the breakdown of the converter losses (Fig. 12a), breakdown of the MOSFETs losses (Fig. 12b) and breakdown of the inductor losses (Fig. 12c). From the Fig. 12a) it can be seen that minimal converter losses are at 12 MHz where the losses between the MOSFETs and the inductor are equal. This point represents the optimal converter design. Regarding the losses of the components of the system, Fig. 12b) shows that, one again,

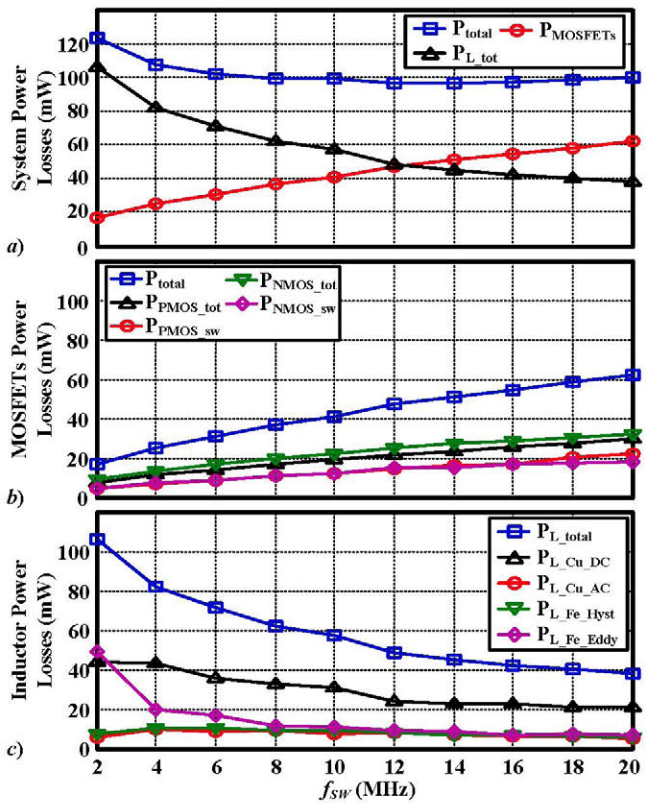

Figure 12. Real MOSFETs - Real Inductor: *a*) Breakdown of the converter losses; *b*) Breakdown of the MOSFETs losses; *c*) Breakdown of the inductor losses.

the losses are balanced between the PMOS and the NMOS, while its switching components are approximately 65% of the losses for the PMOS and 55% for the NMOS. Similar tendency can be observed in Fig. 10 where the impact of MOFET technology is analyzed. The inductor losses, shown in Fig. 12c), have the same behavior as in the first scenario: the losses decrease as the switching frequency increases and the losses are balanced between frequency dependent and the DC losses. Fig. 13 shows component values (Fig. 13a) and the area distribution between the passives (Fig. 13b). As the frequency increases, the needed inductance reduces, while the available area increases, facilitating the inductor implementation.

The comparison of the efficiencies for all four scenarios is presented in Fig. 14. The first scenario with ideal MOSFETs and real inductor ($\eta_{IM\text{-}RL}$ – black, triangles, up) pushes the optimal design at higher frequencies to facilitate the inductor implementation. The second scenario with real MOSFETs and ideal inductor ($\eta_{RM\text{-}IL}$ – blue, squares) has an opposite trend: the optimal design is at low switching frequencies in order to minimize the switching losses. Adding the conduction losses to the inductor while keeping real MOSFETs the optimal design shifts to 4 MHz. finally, adding the core losses to the previous case, real converter behavior is obtained and the optimal design shifts to 12 MHz switching frequency. Additionally, it can be seen in Fig. 14, that the efficiency is not penalized drastically if selected switching frequency is not the optimal. This is coexistent

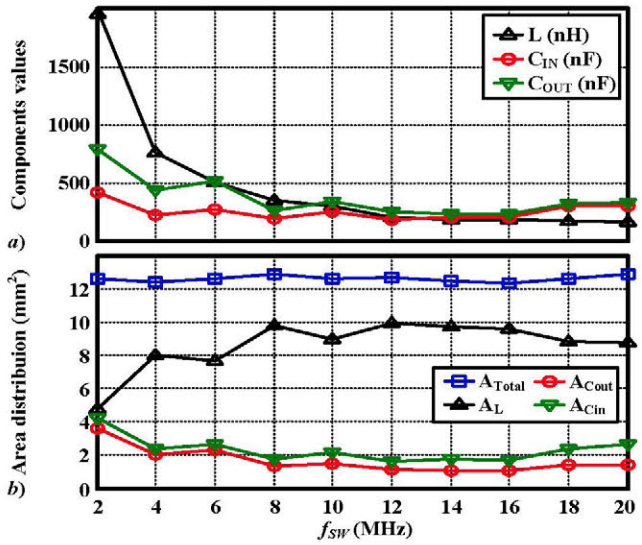

Figure 13. Real MOSFETs - Real Inductor: *a*) Component values; *b*) Area distribution.

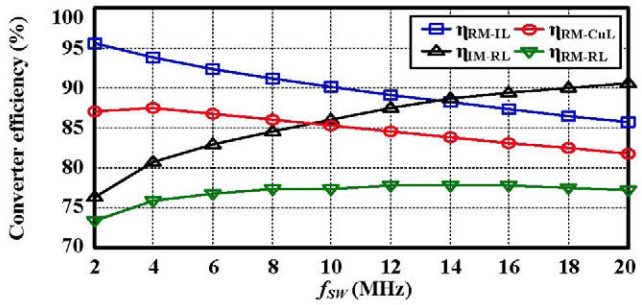

Figure 14. Converter efficiency comparison: real MOSFETs – ideal inductor $\eta_{RM\text{-}IL}$ (blue, squares), ideal MOSFETs – real inductor $\eta_{IM\text{-}RL}$ (black, triangles-up), real MOSFETs –inductor with conduction losses $\eta_{RM\text{-}CuL}$ (red, circles), real MOSFETs – real inductor $\eta_{RM\text{-}RL}$ (green, triangles-down).

with converter losses breakdown, presented in Fig 12a), where it can be seen that total losses of the converter (P_{total} – blue, squares) are relatively flat around its minimum at 12 MHz. this can be used to shift the stress from the passives to the MOSFETs and vice versa: if selected switching frequency is higher than the optimal, the inductor implementation is easier, while the MOSFETs losses are increased; if selected switching frequency is lower than the optimal, MOSFETs losses are smaller, thus the thermal stress is reduced and reliability is increase at the cost of inductor implementation.

Finally, the optimization of the real system has been performed, obtaining the following results for the optimal design: 11.7 MHz optimum frequency; the input and the output capacitors are 175 nF and 245 nF respectively; the inductance is 200 nH and the inductor area is 9.9 mm^2; finally, the widths of MOSETs are 12 mm for PMOS and 14.1 mm for NMOS. The efficiency of the optimal design is 77.5% which is consistent with obtained results presented in Fig. 12. Breakdown of the losses of the system at typical load is presented in Fig. 15 where it is shown that around half of the losses are dissipated in the inductor, while the second half is in the semiconductors.

V. CONCLUTIONS

This study is related to the optimization and analysis of the PwrSoC Buck converter system used to supply in-chip load for automotive application. Due to the complexity of the system and various constrains, multi-variable optimization needs to be employed. In order to reduce optimization time it is needed to use fast mathematical models to estimate power losses with sufficient precision. In addition, due to the dynamic requirements, the optimization needs to be able to analyze dynamic behavior as well.

The optimization of the system has been performed obtaining the design with 77.5% efficiency, operating at 11.7 MHz. the efficiency could be improved implementing the converter with discrete component, but it is penalized due to the full system integration while complying automotive requirements. Further, technology impact analysis of the system has been performed. In the first analyzed case, it is shown that the inductor losses reduce as the frequency is increases. The second case, with real semiconductor technology, has opposite trend: as the frequency increases, the losses increase. As the result of those trends, it can be concluded that improving semiconductors technology will shift optimal design to higher frequencies and improving inductor technology will lower the optimal switching frequency.

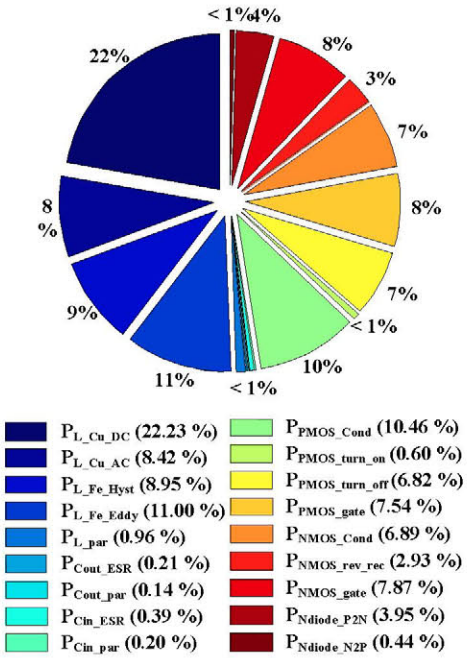

Figure 15. Losses Breakdown: Real system at nominal operating point.

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